

## Patent Abstracts of Japan

PUBLICATION NUMBER : 02009134  
PUBLICATION DATE : 12-01-90

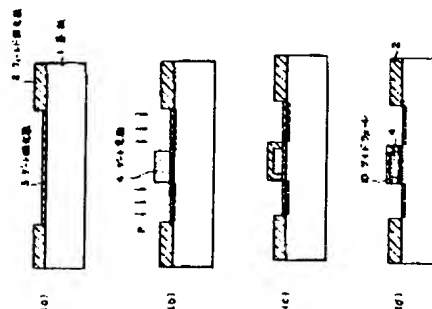
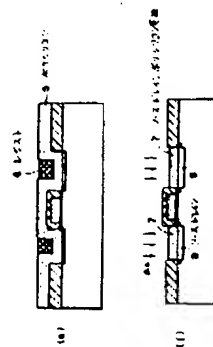
APPLICATION DATE : 28-06-88  
APPLICATION NUMBER : 63157923

APPLICANT : MATSUSHITA ELECTRON CORP;

INVENTOR : KUDO HITOSHI;

INT.CL. : H01L 21/336 H01L 21/28 H01L 29/784

TITLE : MANUFACTURE OF  
SEMICONDUCTOR DEVICE



ABSTRACT : PURPOSE: To lessen overall sheet resistance and achieve planarization of elements by a method wherein ion implantation is carried to polysilicon on the upper portion of source/drain and impurities are diffused from the polysilicon on the source/drain by heat treatment.

CONSTITUTION: A field oxide film 2 and a gate oxide film 3 are formed on a substrate 1. After a gate electrode 4 is formed, ion implantation P is carried out. An oxide film is formed by oxidation. The entire surface as much as the oxide film thickness on the source/drain is etched, and a sidewall 10 is formed with the oxide film in the surrounding of the field oxide film 2 and the gate electrode 4 left. After the natural oxide film on the source/drain is removed, polysilicon 5 is accumulated over the entire surface and a resist 6 is buried in a step recess. Next, the polysilicon is etched with the resist 6 as a mask. Next, ion implantation of As is carried out to the polysilicon, and the source/ drain polysilicon electrode 7 and the source/drain 9 at the substrate side are formed by heat treatment.

COPYRIGHT: (C) JPO